



# Design of Low-Power Reversible Carry Select Adder using D-Latch

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**Abstract:** Most important design parameter in integrated circuit is Power dissipation after speed. Adders are one of the basic fundamental component in such circuit, designing much efficient Adder results in optimizing whole circuit. Due to rapid growth in technology there is a need of fast processing arithmetic unit, so Carry Select Adder (CSLA) is one of the fast processing adder. By observing the CSLA circuitry it is noticed that, further optimization can be achieved in various criteria. Power dissipation results only when bits are lost while processing, as per Landauer's principle,  $kT \ln 2$  heat is dissipated if there is any loss in bit. Since conventional CSLA is designed using irreversible logic gates which it results much more power dissipation but it can be overcome by employing reversible logic to reduce power dissipation till some extent. By using this idea, following paper proposes a efficient technique to design 8-bit CSLA using reversible logic, for this purpose this paper undertakes 8-bit CSLA with D Latch.. This paper evaluates the proposed design in-terms of power, delay, garbage output, quantum cost and number of gates using 90nm CMOS process technology for n-bits. All the works related to proposed design carried in cadence virtuoso tool and by comparing the simulation results and analysis this paper observed that, proposed reversible CSLA using D-latch attains low power dissipation which is equal to 74.1238uW, which shows decrease in 65.175% than irreversible CSLA using D-latch.

**Keywords:** Carry Select Adder (CSLA), Quantum Cost (QC), Garbage Outputs (GO), Fredkin gate (F), Peres Gate (PG), Feynman gate (FG), Reversible D Flip Flop (RDF), Reversible MUX (RMUX), Reversible Ripple carry adder (RRCA), Ripple carry adder (RCA), Reversible full adder (RFA) .

## 1. INTRODUCTION

Most important arithmetic function used widely in all types of digital circuit is adder, it plays vital role in analyzing whole digital hardware. Due to emerging technology several techniques are disclosed to design efficient adder hardware which results in power, delay and area optimization. Since millions of instructions should be performed by any digital device where various addition operations take place so there is need of optimizing above three parameters. But among these constraints power dissipation is one of the major challenging problems since it results various issues. As per Landauer whenever a digital system transmits data from the previous bits then certain amount of energy dissipated, in this case if there is any bit is lost then certain amount of power is leaked. In order to overcome this problem it is necessary to recover those bits which are lost. And also as per CH. Bennett [1, 2] no energy dissipates when system travels from initial to final position. Since this both can be achieved by using reversible logic, it is strongly recommended. There are various adders, Ripple carry adder is one of the efficient adder which is easy to design and also easy to analyze but slow in processing. In order to achieve much more speed using carry look a-head adder is advisable but major drawback of this is consumes more area [3]. By keeping these two major drawbacks, carry select adder is advisable but there is need to optimize in certain aspects because in CSLA either area or delay can be optimize but not both due to utilization multiple RCA pairs to generate partial sum and carry by considering  $C_{in} = 0$  in first stage and  $C_{in} = 1$  in second stage, final results can be obtained by using pairs of multipliers. By keeping this point in view the following paper used CSLA with D-Latch [9] which eliminates RCA's in second stage, where area is optimize but not power dissipation.

The design flow of Reversible CSLA using D-latch explained in this paper is segregated into five sections. Section 2, discuss about existing work, Section 3, it explains proposed design. Section 4, it shows the simulation results of each and every circuit along with the power curve and shows separately overall power to imply power reduction. Section 5, mathematical analysis for n-Bit Reversible CSLA using D-latch. Section 6, conclusion.

## 2. EXISTING WORK

In designing any digital system using reversible logic number of gates, quantum cost and garbage outputs are major parameters for analyzing had defined in [4]. In this paper in section 5 above parameters are analyzed for proposed circuit.



As per the conventional CSLA architecture[8] clearly implies that due to the presence of RCA each and every stage, it occupies much area and also take some time to process operation, since carry as to propagate from previous stage to present stage where it takes some time to propagate.

By keeping this as main point in [5, 6,7] RCA's in second stage of CSLA replaced by binary excess converter (BEC) to achieve lower area and less power dissipation by reducing number of gates in CSLA. Area and power dissipation in CSLA using BEC observed 17.4% and 15.4% reduction comparing with conventional CSLA i.e. in case of 8-bit CSLA using BEC power dissipation is 188.4uW[8]. But major drawback of this design is delay increased slightly comparing with conventional CSLA. Fig 2 explains CSLA with BEC architecture clearly.

Due to this drawback, in [9] designed CSLA using D-latch. In this design style BEC is replaced with D-latch with enable signal. Since D-latch provides output as one when enable signal is one so it is used for load and store operation. In this case output always changes with the change of enable signal. By using this concept, CSLA with D-latch designed in [9]. Fig 3 explains clearly its architecture. In this case input bits are increasing constantly stage by stage.

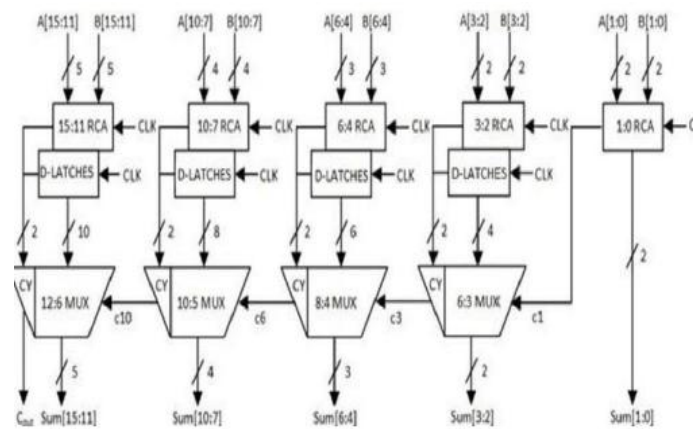


Fig 1. 16-bit Irreversible CSLA with D-latch

It is observed that designed circuit is optimized in terms of area, power and delay comparing with all the above circuits. But after having clear analysis on CSLA with D-latch [9] clearly implies that it can be possible to optimize power much more. By taking this as main criteria, this paper proposes a new design of CSLA using D-latch using reversible logic to optimize power further extent.

In order to design reversible CSLA using D-latch this paper need to design each and every circuitry using reversible logic. Among that D Flip flop is one of the block, in order to have reversible D flip flop this paper used three reversible gates i.e. F gate, and two FG gate from [10] whose garbage output is 2 and quantum cost is 7 and also 2x1 MUX using F gate from [10]. Simulation results are discussed in section 4.

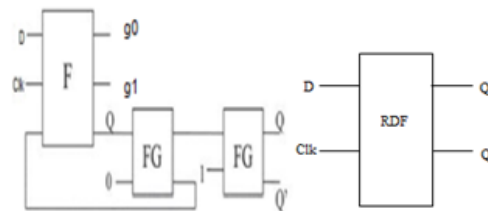


Fig 2. Reversible D Flip Flop (RDF)

### 3. PROPOSED CSLA USING D-LATCH

In order to design proposed circuit, there is need of designing the supporting circuitry in reversible logic. This paper consider [9] as its base paper.

#### 3.1. Reversible Full Adder

Full adder calculates binary data and accounts for carried values in and out. It adds three bits and provides sum and carry. It can be designed in various styles, but in this paper full adder is designed in reversible logic using two PG gates. Simulation results of RFA are discussed in section 4.

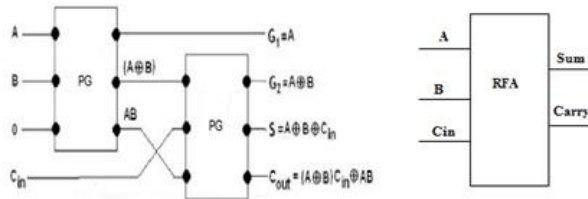


Fig 3. Reversible Full Adder

3.2. Reversible Ripple Carry Adder

It is possible to design logic to add n-bits by using multiple full adders where Cin of each full adder is Cout of previous full adder. Since in this logic circuit the carry ripples from first stage to last stage it is called as RCA. In order to design RRCA this paper cascades RFA, since this paper uses 2-bit RRCA it cascades two RFA. Fig 5 explains detail architecture of 2 bit Reversible RCA.

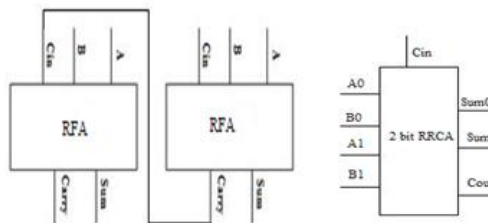


Fig 4 Reversible 2 bit Ripple Carry Adder

3.3. Reversible CSLA using D-latch

Architecture of proposed 8-bit CSA is shown in Fig 6. In order to design this paper used reversible 2-bit RCA, reversible D flip flop and reversible MUX. It consists of four groups of same size RRCA and RDF. Instead of using two irreversible RCA and D latch [9] this paper used one reversible RCA and reversible D latch and also replaced irreversible MUX by reversible MUX which results in power optimization.

In this proposed circuit operation of the given bits are performed in both RRCA and RDF at same time by considering Cin=0 and Clk=1 respectively. This both outputs are feed to reversible MUX. Previous stage Cout is feed to reversible MUX as a selection line, then depending on selection line value RMUX triggers the respective input as output value and it is considered as a sum of the respective group. And the Cout which is obtained in this group from RMUX is considered as a selection line in adjacent group.

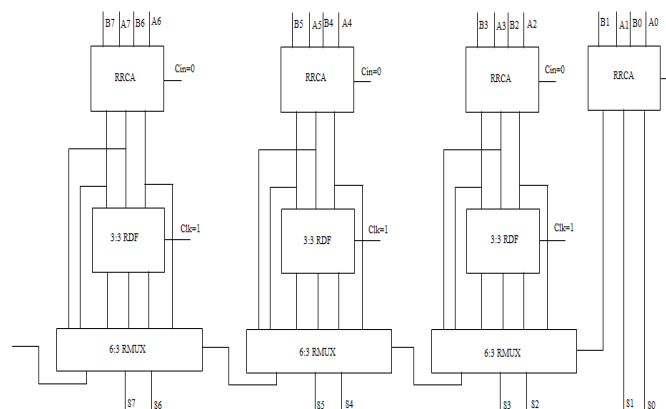


Fig 5. 8-Bit Reversible CSLA using Reversible D-latch

Fig 7 shows internal architecture of group 2 of proposed 8-bit reversible CSLA. In this group addition of two bits A2, B2, A3 and B3 are performed by using two reversible full adders. The third input for both adders are considered as Cin=0. Group 2 consists of three RDF where two RDF are used to store the sums from each RRCA and last one is used to store the carry. Reversible MUX is used to evaluate respective sum and carry values depending on previous stage carry. For this purpose this paper designed 6:3 RMUX i.e. combination of three 2:1 RMUX and also designed 3:3 RDF i.e. combination three RDF where two of them use to store sum values and third one used to store carry.

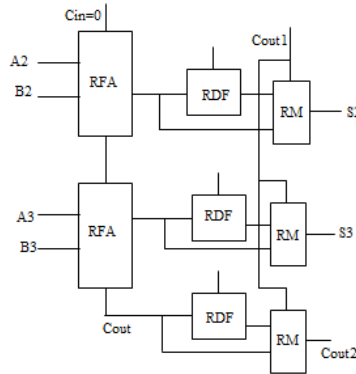


Fig 6 Internal architecture of Group 2

4. SIMULATION RESULTS OF PROPOSED REVERSIBLE CSLA

In these section simulation results of each and every reversible logic used in design is shown which are obtained through cadence virtuoso.

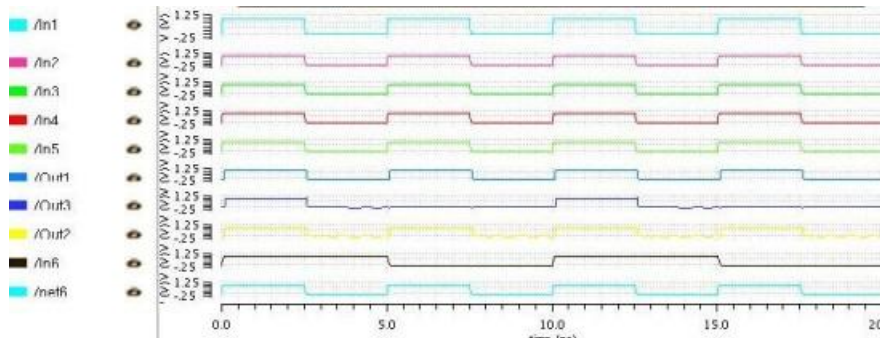


Fig 7. Simulation results of 6:3 Reversible MUX when  $V_{dd}$  is 1v and power dissipation is 4.8uW

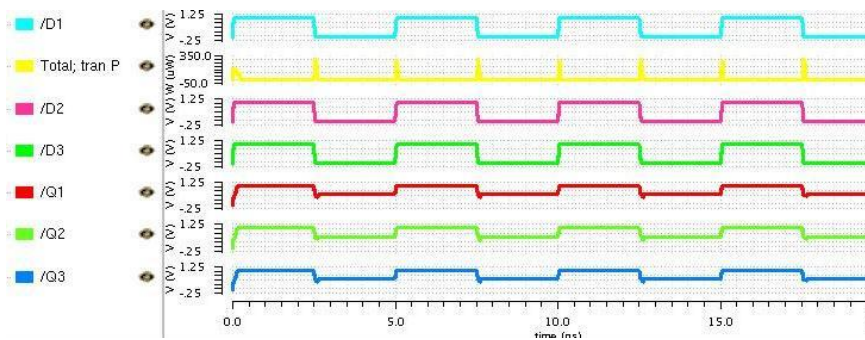


Fig 8. Simulation results of 3:3 Reversible D flip-flop when  $V_{dd}$  is 1V and power dissipation is 8.3uW

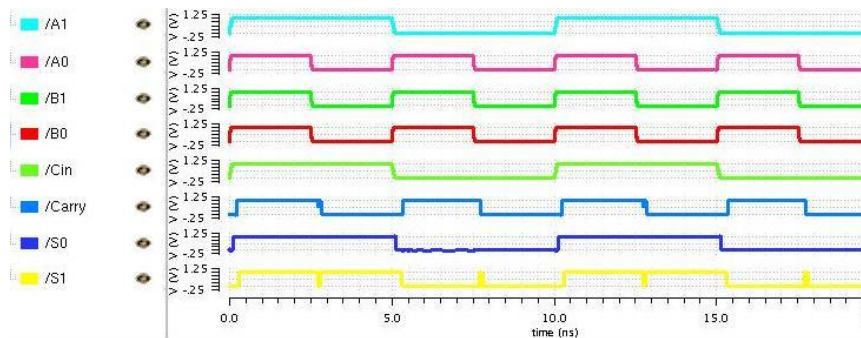


Fig 9. Simulation results of 2 bit Reversible RCA when  $V_{dd}$  is 1V and power dissipation is 10.52uW



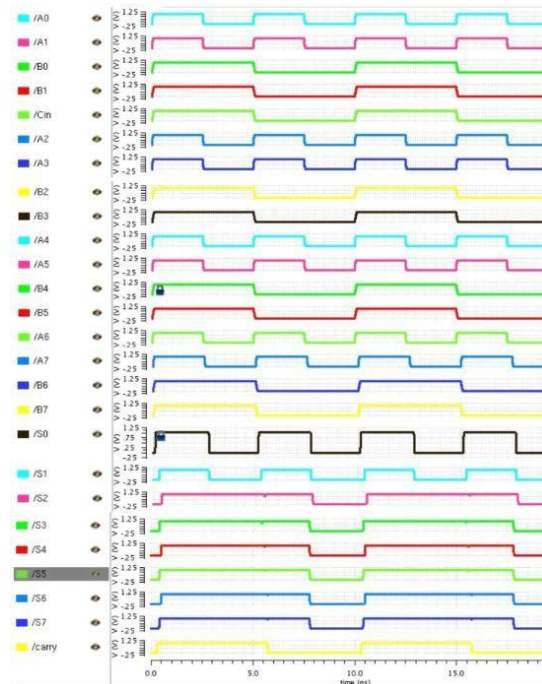


Fig 10. Simulation results of 8 bit Proposed Reversible CSLA using D-latch

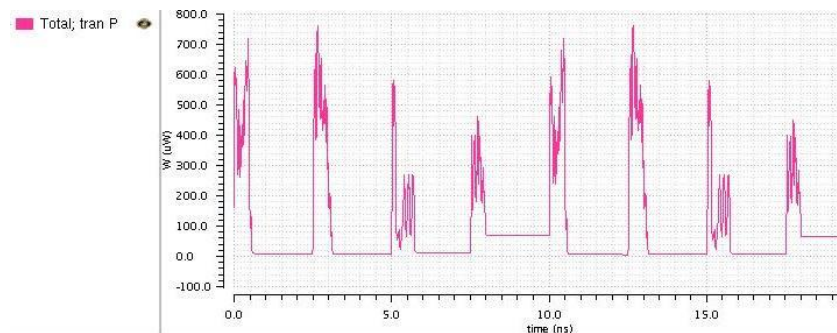


Fig 11. Simulation results of proposed Reversible CSLA power dissipation curve, calculated as 94.58uW

### 5. MATHEMATICAL ANALYSIS FOR N-BIT PROPOSED REVERSIBLE CSLA

#### 5.1 Number of Gates (NOG)

In order to calculate number of gates used, this paper count all gates used in individual cell. To design 6:3 RMUX used three RMUX where each is designed using one F gate. To design 2-bit RRCA used two RFA where each designed using two PG gates. To design 3:3 RDF used three RDF where each designed using one F gate and two FG gate. To calculate NOG for n-bit proposed CSLA following equation deduced

$$\begin{aligned}
 \text{NOG}_{n\text{-bit}} &= n/2\text{NOG}_{\text{RRCA}} + (n-2)/2[\text{NOG}_{3:3\text{RDF}} + \text{NOG}_{6:3\text{RMUX}}] \\
 &= n/2[2 \times \text{NOG}_{\text{RFA}}] + (n-2)/2[3 \times \text{NOG}_{\text{RDF}} + 3\text{NOG}_{\text{RMUX}}] \\
 &= n/2[4] + (n-2)/2[12] \\
 &= 8n-12 \tag{1}
 \end{aligned}$$

#### 5.2. Garbage Output (GO)

Now, the total Garbage Output i.e. unused outputs, required for proposed n-bit reversible CSLA is given by the following expression

$$\begin{aligned}
 \text{GO}_{n\text{-bit}} &= n/2\text{GO}_{\text{RRCA}} + (n-2)/2[\text{GO}_{3:3\text{RDF}} + \text{GO}_{6:3\text{RMUX}}] \\
 &= n/2[2 \times \text{GO}_{\text{RFA}}] + (n-2)/2[3 \times \text{GO}_{\text{RDF}} + 3\text{GO}_{\text{RMUX}}] \\
 &= n/2[8] + (n-2)/2[12] \\
 &= 10n-12 \tag{2}
 \end{aligned}$$



5.3 Quantum Cost (QC)

The quantum cost for n-bit proposed reversible CSLA

$$\begin{aligned}
 QC_{n-bit} &= n/2QC_{RRCA} + (n-2)/2[QC_{3:3RDF} + QC_{6:3RMUX}] \\
 &= n/2[2 \times QC_{RFA}] + (n-2)/2[3 \times QC_{RDF} + 3 \times QC_{RMUX}] \\
 &= n/2[2 \times 2QC_{PG}] + (n-2)/2[3QC_F + 2 \times QC_{FG} + 3 \times QC_F] \\
 &= n/2[16] + (n-2)/2[21+15] \\
 &= 26n-36 \tag{3}
 \end{aligned}$$

5.4 Power Calculation

The total power for proposed n-bit reversible CSLA is given by the following expression

$$P_{n-bit} = n/2P_{RRCA} + (n-2)/2[P_{3:3RDF} + P_{6:3RMUX}]$$

With help of cadence virtuoso this paper calculated power for each and every individual logic block and observed as  $P_{RRCA}=10.52\mu W$ ;  $P_{3:3RDF}=8.34\mu W$ ;  $P_{6:3RMUX}=4.8\mu W$

$$\begin{aligned}
 P_{nbit} &= [n/2[10.52] + (n-2)/2[8.34+4.8]]\mu W \\
 &= [11.9n-13.14]\mu W \tag{4}
 \end{aligned}$$

5.5 Delay Calculation

Total delay for proposed n-bit reversible CSLA is given by the following expression

$$D_{n-bit} = n/2D_{RRCA} + (n-2)/2[D_{3:3RDF} + D_{6:3RMUX}]$$

With help of cadence virtuoso this paper calculated delay for each and every individual logic block and observed as  $D_{RRCA} = 0.28ns$ ;  $D_{3:3RDF}=0.0144ns$ ;  $D_{6:3RMUX}=0.075ns$

$$\begin{aligned}
 D_{n-bit} &= [n/2[0.28] + (n-2)/2[0.0144+0.075]] ns \\
 &= [0.1847-0.0894] ns \tag{5}
 \end{aligned}$$

Model	Power(uW)
Irreversible 8-bit CSLA using D-Latch	160
Proposed Reversible 8-bit CSLA using D-Latch	92

Table 1. Comparison of two models with power

6. CONCLUSION

Power is the main parameter while designing any VLSI circuits. This paper proposed n-bit reversible CSLA using D-latch which consumes less power, as comparing with irreversible CSLA using D-latch [9]. Proposed novel reversible CSLA has  $8n-12$  number of gates and power consumption is  $[11.9n-13.14] \mu W$ . It means proposed n-bit reversible CSLA power reduction is reduced by 66% compared with [4]. Garbage output, quantum cost and delay of proposed n-bit CSLA is  $10n-12, 26n-36, [0.1847-0.0894] ns$  respectively. Design and simulations are performed using cadence 90nm technology.

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